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EXAMINER	
OLANIRAN, FATIMAT O	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,804	BOOR, STEVEN E.	
	Examiner	Art Unit	
	Fatimat O. Olaniran	4178	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-24* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *all*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-9, 11-12 and 14-16 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 15-24 of copending Application No. 10797507. This is a provisional obviousness-type

double patenting rejection because the conflicting claims have not in fact been patented.

Application claim 1 with additional limitations "...a transducer assembly comprising: a housing having an acoustic seal; a transducer for coupling acoustic energy between an outside of the housing and an inside of the housing and a hybrid circuit partially enclosed within the housing..." claims all the limitations of co-pending Application claim 15 (10797507). Although the conflicting claims are not identical, they are not patentably distinct from each other because both the claims of instant application and the claims of co-pending Application (10797507) are almost the same in scope although co-pending Application claim 15 (10797507) omits some limitations in claim 1. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify co-pending Application claim 15 (10797507) with those additional limitations so as to obtain claim 1 as claimed.

Allowance of claim 1 would result in an unjustified time-wise extension of the monopoly granted for the invention defined by co-pending Application claim 15. Therefore, provisional obviousness-type double patenting is appropriate because the conflicting claims have not in fact been patented.

Claim 2 corresponds to co-pending application 10797507 claim 16

Claim 3 corresponds to co-pending application 10797507 claim 17

Claims 4, 5, 6, 7, 8 corresponds to co-pending application 10797507 claim 18

Claim 9 corresponds to co-pending application 10797507 claim 19

Claim 11 with additional limitations "...assembling the buffer circuit in an acoustically sealed housing, a portion of the buffer circuit accessible from outside the housing..." claims all the limitations of co-pending Application claim 20 (10797507). Although the conflicting claims are not identical, they are not patentably distinct from each other because both the claims of instant application and the claims of co-pending Application (10797507) are almost the same in scope although co-pending Application claim 20 (10797507) omits some limitations in claim 11. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify co-pending Application claim 20 (10797507) with those additional limitations so as to obtain claim 11 as claimed.

Allowance of claim 11 would result in an unjustified time-wise extension of the monopoly granted for the invention defined by co-pending Application claim 20. Therefore, provisional obviousness-type double patenting is appropriate because the conflicting claims have not in fact been patented.

Claim 11 corresponds to co-pending application 10797507 claims 21

Claim 12 corresponds to co-pending application 10797507 claim 22

Claim 14 corresponds to co-pending application 10797507 claim 23

Claims 15 and 16 corresponds to co-pending application 10797507 claim 24

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-3, 9-12, 15, 17 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of Madaffari et al. (2002/0090102).

Claim 1, Levitt discloses a transducer for coupling acoustic energy between an outside of the housing and an inside of the housing (Fig. 2: microphone 57, col. 4 line 64); and a hybrid circuit partially enclosed within the housing (Fig. 2), the hybrid circuit a first input circuit for coupling a signal from the transducer (Fig. 2: element 58); a filter network (Fig. 2: element 64) coupled to the first input circuit; an output circuit coupled to the filter network (col. 5 line 7-11); a tuner for adjusting the filter network(Fig. 2; 84 :EEPROM, tri-state switches, 85-86); and a controller for altering a value of the tuner(Fig. 1 host controller), the controller having a second input on a portion of the hybrid circuit external to the housing (Fig. 1:element 124 EEPROM socket), whereby a tuning signal coupled to the second input is used to adjust the tuner, thereby changing a characteristic of the filter network (col. 2 line 49-51).

Levitt does not disclose a housing having an acoustic seal.

Madaffari discloses a housing having an acoustic seal (Fig. 2, paragraph 15 line 13-15).

Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the housing of Madaffari in order to protect the circuit from EMI and other interferences.

Claim 2 analyzed with respect to claim 1, Levitt further discloses, wherein the controller retains a setting upon receiving the tuning signal (col. 4 line 38-43).

Claim 3 analyzed with respect to claim 1, Levitt further discloses, wherein the portion of the hybrid circuit external to the housing is permanently removed after the controller receives the tuning signal (col. 8 line 25-29 the computer is disconnected after programming).

Claim 9 analyzed with respect to claim 1, Levitt further discloses wherein the second input is coupled to a biasing element, the biasing element maintaining a state after receiving the tuning signal (col. 5 line 34-37).

Claim 10 analyzed with respect to claim 1, Levitt further discloses wherein the transducer is a microphone (Fig. 2: element 57).

Claim 11, Levitt discloses a portion of the buffer circuit accessible from outside the housing (Fig. 1; element 24);
providing a desired response characteristic for the buffer circuit (col. 6 line 65-67);

measuring an initial response characteristic of the buffer circuit (col. 6 line 68); comparing the desired response characteristic to the initial response characteristic (col. 7 line 1-2); determining an adjustment using the comparison, the adjustment for reducing a difference between the desired and initial response characteristics (col. 7 line 1-2); transmitting a signal to a selector circuit in the buffer circuit (col. 7 line 6-8); and tuning an adjustable filter coupled to the selector circuit (col. 7 line 11-12), the adjustable filter for modifying the initial response characteristic (col. 7 line 65-67). Levitt does not disclose assembling the buffer circuit in an acoustically sealed housing. Madaffari discloses assembling the buffer circuit in an acoustically sealed housing (Fig. 2, paragraph 15 line 13-15).

Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the housing of Madaffari in order to protect the circuit from EMI and other interferences.

Claim 12 analyzed with respect to claim 11, Levitt further discloses removing the portion of the buffer circuit accessible from outside the housing, the portion used in transmitting the signal to the selector circuit (col. 8 line 25-29, the computer is disconnected after programming.)

Claim 15 analyzed with respect to claim 11, Levitt further discloses wherein the tuning the adjustable filter further comprises biasing the selector circuit with a biasing component (col. 5 line 34-40).

Claim 17 analyzed with respect to claim 15 and 11, Levitt further discloses wherein the biasing component is an electrically erasable programmable read-only memory (EEPROM) (col. 2 line 49-52).

Claim 20, Levitt discloses, a transducer assembly having a transfer function of an acoustic energy to electrical energy comprising

a substrate having a first portion inside the housing (Fig. 2, col. 4 line 65) and a second portion extending outside the housing (Fig. 1, host controller); and

a circuit disposed on the substrate for receiving a signal corresponding to acoustic energy received at the acoustic port (Fig. 2 col. 4 line 66-68),

whereby the transfer function of the miniature transducer assembly can be altered by a signal injected at the second portion of the substrate (col. 4 line 38-42). Levitt does not disclose a housing comprising a first molded piece having an acoustic port;

a second molded piece coupled to the first molded piece.

Madaffari discloses a housing comprising a first molded piece having an acoustic port (Fig. 2; element 52); a second molded piece coupled to the first molded piece (Fig. 2; element 42).

Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the housing of Madaffari in order to protect the circuit from EMI and other interferences.

Claim 21 analyzed with respect to claim 20, Levitt further discloses wherein the second portion of the substrate is removably attached to the first portion (Fig. 1; EEPROM socket).

Claim 22 analyzed with respect to claim 20, Levitt further discloses wherein the circuit comprises a component for receiving the signal, the component operable to retain a programmed state after receiving the signal (Fig. 4 EEPROM col. 2 line 48-50).

Claim 23 analyzed with respect to claim 22 and 20, Levitt further discloses wherein the component is coupled to one of a resistor ladder network and a decoder (Fig. 4; element 148, col. 10 line 60-61).

Claim 24 analyzed with respect to claim 20, Levitt further discloses wherein the component is one of a zener-zap diode, an electrically erasable programmable read only memory (EEPROM), a poly-silicon fuse and a laser trimmable hybrid resistor (Fig. 4 EEPROM col. 2 line 48-50).

6. Claim 4-8 and 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of Madaffari et al. (2002/0090102) in further view of Killion (5602925).

Claim 4 analyzed with respect to claim 1, Levitt in view of Madaffari does not disclose wherein the tuner is a ladder network, the ladder network adjustable by activating or

deactivating a semiconductor device between an element of the ladder network and a signal ground connection.

Killion discloses wherein the tuner is a ladder network, the ladder network adjustable by activating or deactivating a semiconductor device between an element of the ladder network and a signal ground connection (Fig. 6. col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt in view of Madaffari with the ladder network and semiconductor of Killion in order to save space when implementing the circuit and in order to have a silicon based transistor that can be implemented with the rest of the circuit.

Claim 5 analyzed with respect to claim 4 and claim 1, Killion further discloses wherein the ladder network comprises resistors (Fig 6).

Claim 6 analyzed with respect to claim 5, 4 and 1, Killion further discloses wherein the resistors have a nominal value of 5.5k ohms. However, it would be obvious to one of ordinarily skill in the art at the time the invention was made to set the value of the resistive element to 5.5k ohms in the course of circuit design so as to limit current applied or as necessary.

Claim 7 analyzed with respect to claim 4 and 1, Levitt further discloses wherein the ladder network comprises, capacitors (Fig. 4, col. 10 line 66-67).

Claim 8 analyzed with respect to claim 4, Killion further disclose wherein the semiconductor device is a field effect transistor (FET) (Fig.6 col. 6 line 7-9).

Claim 14 analyzed with respect to claim 11, Levitt in view of Madaffari do not disclose wherein the tuning the adjustable filter further comprises activating a semiconductor device between an element of a ladder network and a ground connection.
Killion discloses wherein the tuning the adjustable filter further comprises activating a semiconductor device between an element of a ladder network and a ground connection (Fig. 6. col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt in view of Madaffari with the ladder network and semiconductor of Killion in order to save space when implementing the circuit and in order to have a silicon based transistor that can be implemented with the rest of the circuit.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of Madaffari et al. (2002/0090102) and in further view of Advani et al. (4926459).
Claim 16 analyzed with respect to claim 15 and claim 11, Levitt in view of Madaffari does not discloses, wherein the biasing component is a zener-zap diode.
Advani discloses wherein the biasing component is a zener-zap diode (Fig. 3; element 106, col.7 line 46-47). Therefore it would be obvious to one ordinarily skilled in the art at

the time the invention was made to modify the circuit of Levitt with a zener-zap diode as taught by Advani in order to utilize the breakdown characteristic of diodes.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of in view of Madaffari et al. (2002/0090102) in further view of Suzuki (5365768).

Claim 18 analyzed with respect to claim 15 and 11, Levitt in view of Madaffari do not disclose wherein the biasing component is a polysilicon fuse.

Suzuki discloses wherein the biasing component is a polysilicon fuse (col. 6 line 56-59). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the tuning circuit of Levitt in view of Madaffari with a polysilicon fuse, as taught by Suzuki so that the melting or nonmelting of the polysilicon fuse can be used as a digital memory (Suzuki col. 8 line 12-13).

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of Madaffari et al. (2002/0090102) in further view of Lai (6229428).

Claim 19 analyzed with respect to claim 15 and claim 11, Levitt in view of Madaffari does not disclose wherein the biasing component is a laser trimmable hybrid resistor.

Lai discloses wherein the biasing component is a laser trimmable hybrid resistor (col. 1 line 65-66 and col. 2 line 48-49). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the tuning circuit of Levitt in view

of Madaffari with a laser trimmable hybrid resistor, as taught by Lai in order to have a resistor that can still be adjusted after the circuit has been assembled.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fatimat O. Olaniran whose telephone number is 571-270-3437. The examiner can normally be reached on M-F Alt F off 8:30-6 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hai Tran can be reached on 571-272-7305. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FO

HAI TRAN
PRIMARY EXAMINER